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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/845,874	04/30/2001	Peter Kliegelhofer	GR 99 P 1649	4738

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EXAMINER	
CHU, GABRIEL L	
ART UNIT	**PAPER NUMBER**
2114	7

DATE MAILED: 04/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/845,874	KLIEGELHOFER ET AL.	
	Examiner	Art Unit	
	Gabriel L. Chu	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 February 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

2. Claims 1-4 are rejected under 35 U.S.C. 102(b) as being anticipated by US 4748594 to Iida. Referring to claim 1, Iida discloses an operating method, which comprises the steps of: providing a memory device for storing data (From figure 2, element 200.); storing the data in the memory device a plurality of times resulting in originally stored data (From line 59 of column 4, "In FIG. 2, three sets of the same information are written at different addresses a.sub.1, a.sub.2 and a.sub.3, respectively, of the memory 200."); and reconstructing the originally stored data as required from the data stored a plurality of times taking into account a direction of any memory content changes which arise (From line 10 of column 3, "means for performing a majority logic operation on the sets of the read-out information, and means for taking out correct information from the majority logic operation performing means.").

Referring to claim 2, Iida discloses during the reconstruction of the data originally stored in the memory device, subjecting mutually corresponding bits of the data stored a plurality of times to a Boolean operation (From line 34 of column 4, "a majority logic operation circuit (AND gates 110, 111, 112, and an OR gate 113)".).

Referring to claim 3, Iida discloses configuring the memory device to store the data, that are to be stored in the memory device, automatically in the memory device a plurality of times From line 59 of column 4, "In FIG. 2, three sets of the same information

are written at different addresses a.sub.1, a.sub.2 and a.sub.3, respectively, of the memory 200.").

Referring to claim 4, Iida discloses providing additional information dependent on the data being stored in the memory device (From line 59 of column 4, "In FIG. 2, three sets of the same information are written at different addresses a.sub.1, a.sub.2 and a.sub.3, respectively, of the memory 200."); and reconstructing the originally stored data as required from the data stored a plurality of times and the additional information (From line 10 of column 3, "means for performing a majority logic operation on the sets of the read-out information, and means for taking out correct information from the majority logic operation performing means.").

Response to Arguments

3. Applicant's arguments filed 10 February 2004 have been fully considered but they are not persuasive. Regarding Applicant's argument that Iida does not disclose reconstructing the originally stored data taking into consideration a direction of any memory content change that may occur, stated one more time for clarity and emphasis, from line 59 of column 4, "In FIG. 2, three sets of the same information are written at different addresses a.sub.1, a.sub.2 and a.sub.3, respectively, of the memory 200." Further, from line 10 of column 3, "means for performing a majority logic operation on the sets of the read-out information, and means for taking out correct information from the majority logic operation performing means." Examiner has provided data stored in the memory a plurality of times: the same information is written at different addresses at least two times, constituting a plurality of times, constituting "original data". This data,

taken along with the third time, qualifying as "additional data", is read into a majority voting circuit to "take into account a direction of any memory content change which arises". If such a change occurs, this majority voting circuit votes on the change and reconstructs, i.e., constructs again, the originally stored data "as required".

Conclusion

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gabriel L. Chu whose telephone number is (703) 308-7298. The examiner can normally be reached on weekdays between 8:30 AM and 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W. Beausoliel, Jr. can be reached on (703) 305-9713. The fax

phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

gc

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